

Requirement for Robust Capacitors in High Density Power Converters

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ABSTRACT

Power supply designers are faced with complex component size and part shape issues in order to minimize circuit board land area and maximize cubic space efficiency. Packing density and logical layout of the topology is often made difficult because of the mechanical and electrical shortcomings of the components. Chip capacitors are perhaps the most fragile components in the power system, being easily damaged by external physical events. Capacitor damage often occurs from process events such as pick & place, part soldering, temperature shock, and circuit board flexing during circuit board assembly. Less obvious reasons for damaged capacitors are location of chip capacitors near board edges, proximity to large heat sinks, pad size and solder fillet mass. Large chip capacitors are very fragile to mechanical shock of any kind, so it is often necessary to use multiple small units or employ special lead frame chip carriers to avoid cracking. Field problems related to chip component fragility cause converter designers to add cost in terms of component safety margin allowance and special handling and housing for the chip components on the board.

Multilayer Polymer (MLP) chip capacitors (see Fig. 1), based upon the newest low shrinkage PET polymer dielectric, offer a physical strength and mechanical flexibility that avoids cracking failures on the circuit board. Their stability under voltage and current loads provides a quality alternative to MLC capacitors in high current power conditioning circuits.

CONVERTER MANUFACTURER ISSUES

High-density power converter manufacturers have learned about capacitor component failure mechanisms through costly yield losses in the factory. Even after the power converter is in the field, once under application stress, additional component related thermo-mechanical and electrical weaknesses must be taken into account. Temperature cycling in use can cause cracking of the chip capacitor due to thermal coefficient of expansion difference between the component and circuit board material. The use of hard-set thermally conductive potting compounds and super thin circuit boards has exasperated these issues.

High in-rush current can cause a chip to break if its piezoelectric property is poor or if the dv/dt rating of the part is inadequate for spike currents on the voltage bus. Since all dielectric systems are not perfectly stable over voltage, temperature and frequency changes, worst case conditions must be planned for. At low temperature, some popular chip capacitors have very high ESR (higher by several orders of magnitude) com-

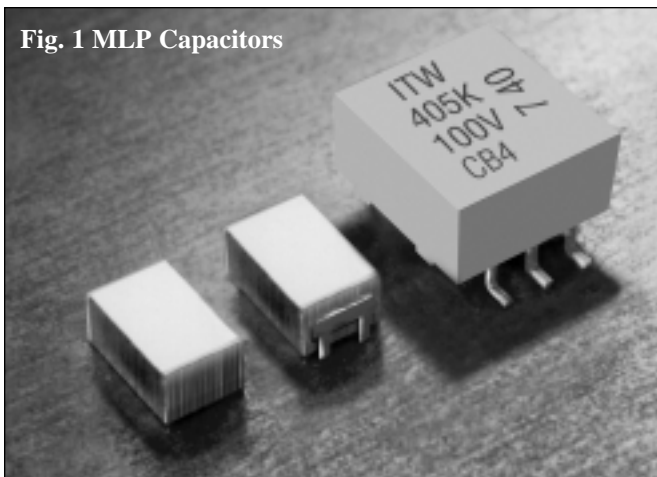


Fig. 1 MLP Capacitors

pared to room temperature specifications. Cold start problems can result in cracked and shorted capacitors. At high frequency, the dissipation factor of all dielectrics rises, resulting in increasing ESR that limits attenuation property and can cause heat losses. Increasing AC ripple current on the capacitor causes certain dielectrics to increase in ESR to potentially run away explosive condition. Even simple DC bias on popular MLC dielectrics causes significant capacitance drop that can reduce the ripple current and load handling capability of the component. Finally, age and time have effects (normally worsening) on the capacitors that can become significant in a few short weeks. The new demands on DATACOM producers to match the 10 to 20 year life of the TELECOM producers with 100% up-time products changes component selection criteria. It must be remembered a 2000 hour product means only 83.3 days. The extrapolation to 10 years life is a far reach for most capacitor systems that are subject to electrical degradation with time.

In high frequency switching power converters, the input and output filtering function is handled by large discrete capacitors, usually configured in multiples (banks) of parallel units to achieve power handling and ripple current control. In PWM and resonant control DC-to-DC converters, the reactive input filter section requirements have usually been underestimated due to the reflected, harmonic RFI created internally, and from externally generated pulse events appearing on the system bus. Many DC-to-DC converters are under-filtered when it comes to RFI control and must be decoupled externally. Because the input filter section sees a moderate to low series current, normally one or two amps at 48 volts, a small valued capacitor can be used on the input, provided the dissipation factor is low enough to efficiently sink the ripple current, and the high frequency impedance is low enough to bypass reflected RFI. These capacitors can be either X7R ceramic or MLP film capacitors. Both types are built on a "stacked" layer construction that features very low impedance and ESR extending well beyond the switching frequency of high-density converters. Developments to provide higher capacitance values in small package sizes have now led to the use of these low ESR capacitors in output filters where the load currents are at least ten times higher than on the higher voltage input bus. The selection of an electrostatic capacitor (ceramic or film) can improve the reliability of the power system to a level where the tantalum electrolytic capacitors typically used can either be reduced in number or eliminated from the output

filter. Tantalum capacitors can have very high dissipation factor, which can lead to self-heating and failure in high ripple current applications such as with TELECOM boards and CPUs.

The current handling aspect of electrostatic capacitors is fundamental to their reliability in the power train. On the input side, the in-rush current ratings are important due to the input voltage level and high-energy pulses carried on the bus. The capacitor's instantaneous current handling capability has a direct relationship on the dv/dt rating (or dv/dt rating per individual layer in the stack), in combination with the capacitance value (or number of parallel stacks). These dv/dt ratings are not readily available in product literature and can vary greatly over temperature and frequency. A working knowledge of in-rush current effects under typical converter usage parameters is paramount in understanding the reliability of the ceramic and film capacitors presently used on the input filter section. Since the input section is normally 48 volts or higher, any misapplication can produce a high-energy failure, resulting in a "hard short". The output filter section typically features high ripple currents at low bus voltage. The ripple current ratings of the capacitors vary widely depending upon the component temperature rise allowed, but are directly influenced by the high frequency ESR and ESL of the part (or bank of parts). Knowledge of the high frequency dissipation factor levels of ceramic, film and tantalum capacitors and how these relate to ripple current handling allows the design engineer to better determine which capacitor system is most suitable in the application (see Fig. 2).

A short circuit within parallel mounted capacitors on a power train most often exhibits a disastrous failure mode (see Fig. 3). This is true both on the input, in the series resonant tank and on the output filter of converters. Popular electrostatic capacitors featuring high capacitance values are either multilayer ceramic or multilayer polymer. While also popular, electrolytic capacitors such as tantalum capacitors have relatively high dissipation factor and are limited in operating fre-



Fig. 3 Ceramic Capacitor Short Circuit Failure

Selected Value	Data on Typical Capacitor Types		Dissipation Factor		ESR @ 25°C (100KHz)	Ripple Current (100KHz)
	DCV	(1KHz)	(100KHz)			
Aluminum 1000µf	6	10.0%	15.70%	0.025	1.0	
Tantalum 680µf	6	6.0%	9.80%	0.023	3.0	
OS-CON 330µf	6	6.0%	4.10%	0.020	3.5	
Ceramic - X7R 10µf	100	2.5%	0.94%	0.015	6.0	
MLP-PET 10µf	100	1.0%	0.69%	0.003	14.1	
		Spec.	Actual	Spec.		

quency. Tantalum capacitors are also subject to shorting especially at elevated voltage and high di/dt conditions. For these and other reasons next generation capacitor technologies such as Paktron's MLP (Multilayer Polymer) capacitors are showing increased use as output filter capacitors where the energy levels are high and low ESR is required above 100 kilohertz.

CAPACITOR TECHNOLOGIES

A. Tantalum Capacitors

Tantalum capacitors are constructed with a very porous anode made with tantalum powder (see Fig. 4). This powder is pressed into a pellet form with a tantalum wire inserted. The pellet is sintered to allow for contact growth between the individual particles. This results in a porous structure, which electrically connects all the tantalum particles to one another as well as to the tantalum wire. The dielectric in a tantalum capacitor is formed on the exposed surfaces of the tantalum through electro-chemical treatment. The resulting film layer (dielectric) is extremely thin and the total surface area throughout the porous structure is extremely high allowing for the production of very high capacitance values.

Makers of tantalum capacitors are under pressure to reduce the ESR of the parts for extended use at high frequency, and to be more reliable on high current DC bus. Several major developments are under way to replace the manganese dioxide cathode system with a conductive polymer electrolytic cathode. Difficulties and schedule delays with these efforts have led to parallel developments to extend the capacitance values of the current manganese dioxide based products in order to reduce the ESR of the capacitors. The effort to reduce the ESR by simply increasing capacitance value has driven producers to package multiple anodes in one molded device (see Fig. 5). Unfortunately, the denser anodes tend to cause the dissipation factor to increase and the adoption of multiple anodes runs contrary to quality and reliability of design principles.

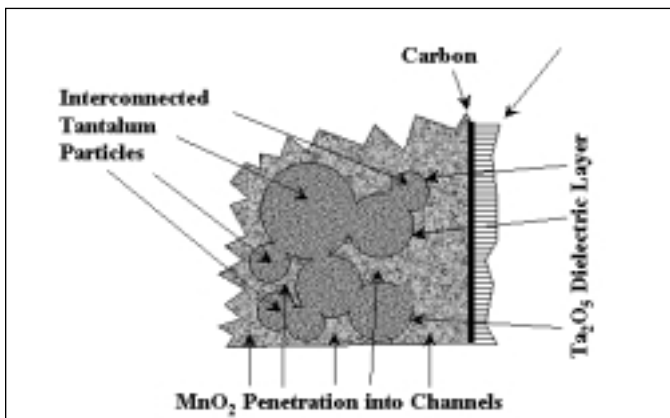


Figure 4 Tantalum Capacitor Construction

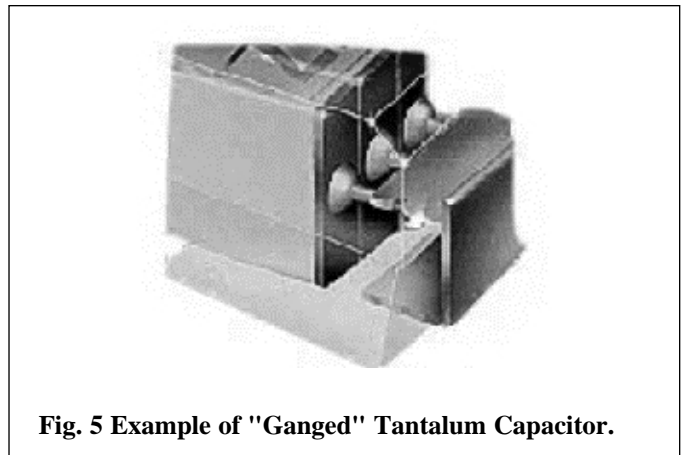


Fig. 5 Example of "Ganged" Tantalum Capacitor.

B. Multilayer Ceramic Capacitors

The typical ceramic capacitor is multilayer ceramic (MLC). This type of capacitor is a monolithic block composed of ceramic material containing two sets of offset interleaved electrodes that are exposed on opposite edges of the laminated structure (see Fig. 6). After laminating, this structure is fired at high temperature to produce a monolithic block. After firing, conductive termination is applied to the opposite ends in order to make contact to the exposed electrodes. This conductive termination material typically consists of a nickel barrier layer and a tinned coating to facilitate soldering.

The multiple layers and high dielectric constant ceramic allows for the production of relatively high capacitance values per unit size. These types of capacitors are easily surface mountable and have found wide acceptance in signal level applications. Complications occur when trying to use MLC capacitors in applications requiring both "high" capacitance and "high" voltage at the same time which many times results in "cracked" layers (see Fig. 7). In contrast to MLP capacitors with its thousands of stacked layers, MLC capacitors consist of anywhere from only 20 to several hundred layers (in multi stack designs).

In the input filter section, the dv/dt or in-rush current capability of the device should always be a primary consideration.

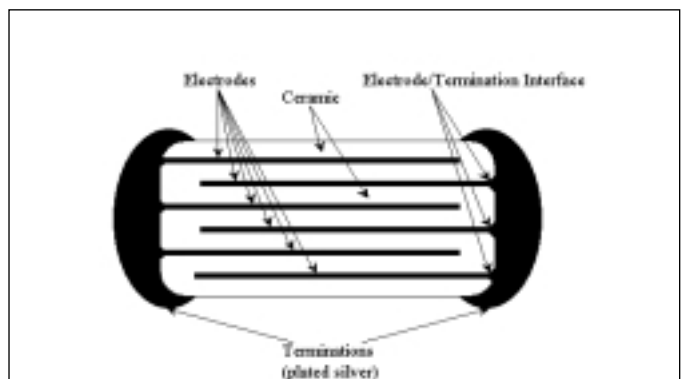


Fig. 6 Ceramic Capacitor Cross Section

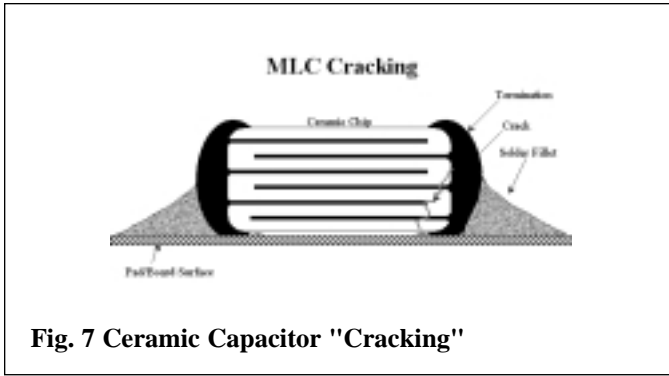


Fig. 7 Ceramic Capacitor "Cracking"

Current in-rush is usually a problem at system startup. Applying 48 volts with a high di/dt can cause an instantaneous failure with certain types of capacitor. It is widely known that ceramic capacitors can fail in the short circuit mode while MLP capacitors will remain in an operational state after a "clearing" event.

In recent years, ceramic capacitor manufacturers have seen an accelerated escalation of the price of palladium metal to levels exceeding the price of gold. Palladium is a very stable, reasonably ductile, and non oxidizing noble metal which was found in virtually all multilayer ceramic (MLC) capacitors' electrode and conductive termination systems. The MLC industry is actively seeking to replace the precious metal palladium (and palladium/silver alloy) with nickel or copper base metals. This provides an opportunity for cost abatement but the simple replacement of the metal has not proven to be easy. In fact, this development has been an ongoing project within the ceramic capacitor industry for decades. It has been found that, no matter how innovative the engineering; chip capacitors made with base metal electrodes tend to be more fragile and less stable than their noble metal counterparts are (see Fig. 8). It should be noted in this magnified view that the electrode plates are highly disassociated (fragmented). While a certain degree of "lacy" electrodes is desirable (for a more monolithic block), excessive discontinuity will lead to reduced pulse handling, increased ESR and the potential for "hot spots" that significantly decrease reliability.

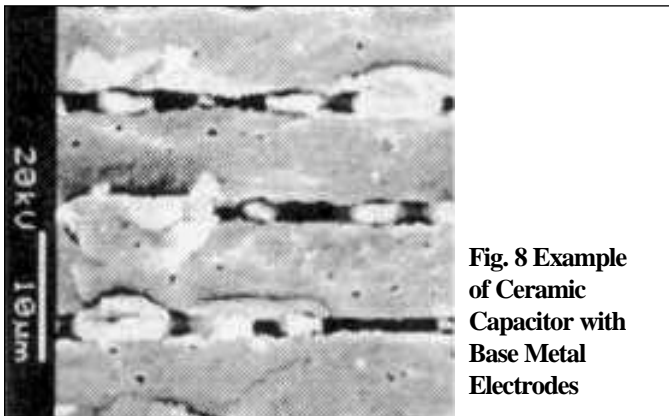


Fig. 8 Example of Ceramic Capacitor with Base Metal Electrodes

C. Metallized Film Capacitors

Metallized film capacitors consist of thin film layers of polymer based material upon which a metal has been vapor deposited to act as electrode plates. Many designers who use metallized film capacitors do not realize that although all film capacitors use the same base capacitor materials, metallized film capacitors are produced by two significantly different base construction technologies that will behave radically different in their applications. One of these technologies is a "wound" construction and the other "stacked" (see Fig 9). "Wound" technology takes two offset lengths of film and rolls an individual cylindrical capacitor. Should the form factor require a modification, the cylinder is flattened and an oval capacitor formed. "Stacked" capacitor technology takes the same two offset lengths of film (or more) and winds the layers together on a large wheel to form a mother capacitor. The mother capacitor has its layers laminated together and is sawed into individual capacitors.

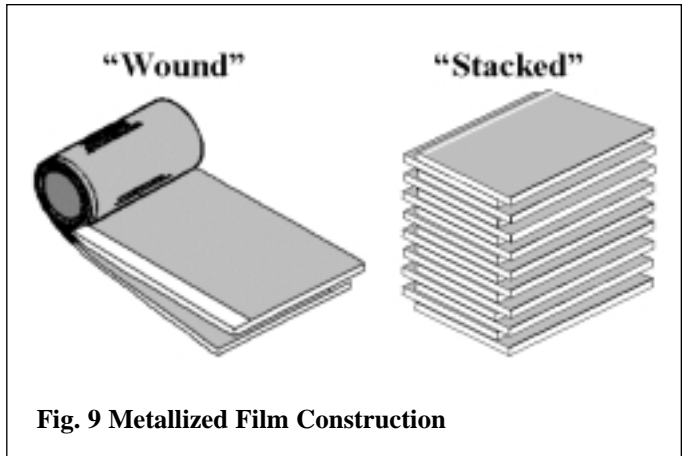


Fig. 9 Metallized Film Construction

"Wound" technology has produced high quality, mass producible product for decades. Unfortunately, it does have several limitations in its use in high-density power converters. The Interleaf Technology construction that is used to produce MLP capacitors is based on "stacked" construction (see Fig. 10).

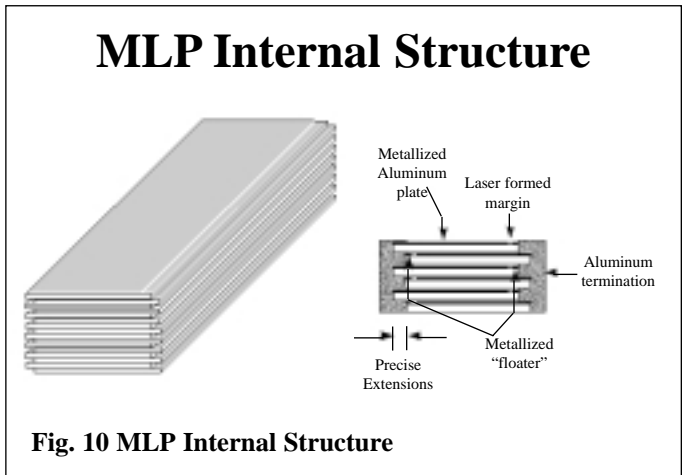


Fig. 10 MLP Internal Structure

The advantages in "stacked" vs "wound" are significant and include such things as lower inductance, lower dissipation factor, lower ESR, higher current handling, better stability, improved volumetric efficiency and being far more conducive to mass production (see Figs. 11 and 12).

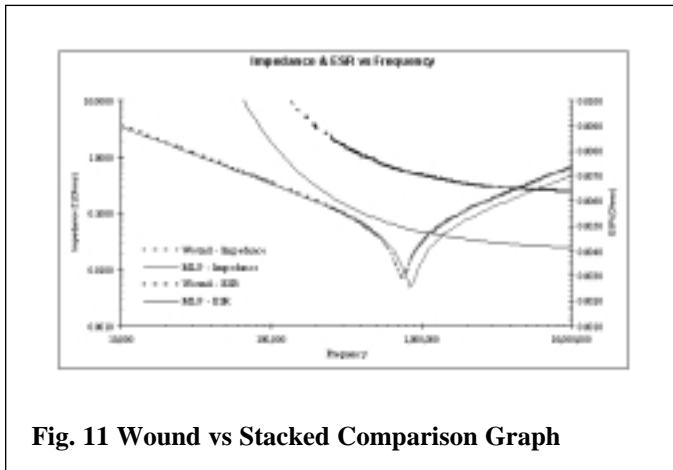


Fig. 11 Wound vs Stacked Comparison Graph

Parameter	Worst Case Sample Readings	
	Stacked	Wound
ESR @ 500KHz	5.29mΩ	7.74mΩ
Resonance Freq.	853KHz	743KHz
Eqv. L	3.1nH	6.9nH
Eqv. R	4.86mΩ	7.35mΩ

Typical reading taken on 4.7mfd 100vdc units

Fig. 12 Wound vs Stacked Comparison Table

The MLP style capacitor employs metallized electrode construction. These electrode plates are composed of 100-300 angstroms of vapor deposited base metal resulting in 1.0-5.0 ohms/square of plate resistance (100 angstroms = 0.0000003937"). The Interleaf Technology construction overcomes the "high" surface resistivity of the deposited aluminum electrodes by stacking thousands of layers of plate resistance in parallel thereby producing an extremely low effective total resistance (Rt) for the capacitor (typically under 10 milliohms). For example, a capacitor could have 1.0 ohms per layer of DC resistance, but because there can easily be 2,000 paralleled stacks within the capacitor, the total resistance of the electrode plates would only be 5.0 milliohms (see Fig. 13).

The stacking of thousands of layers of very thin film dielectric also allows for the production of relatively high capacitance values and associated high current ratings in small package sizes. Depending upon the capacitor's rated voltage, the dielectric thickness of each of these layers can range from 0.6 micron to 8.0 microns, with a micron being approximately 1/10,000 the

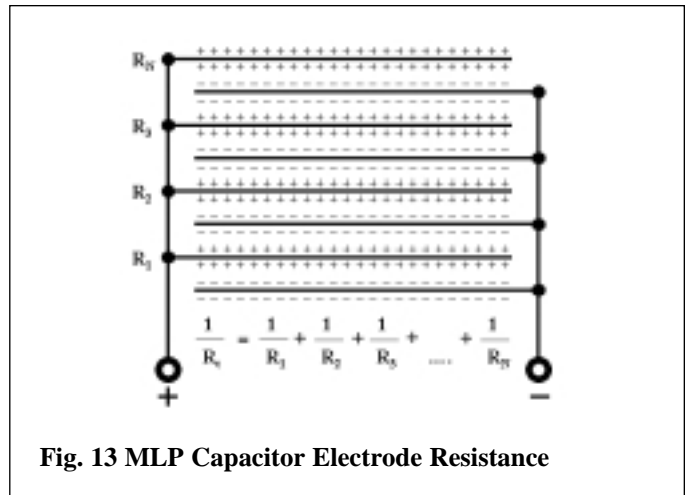


Fig. 13 MLP Capacitor Electrode Resistance

thickness of a human hair (1 micron = 0.000040"). Stacking 2,000 layers of 1 micron thick dielectric results in a basic capacitor block thickness of only 2.03mm (0.080").

Metallized film capacitor manufacturers have been under intense pressure to produce a more thermally resilient chip component, one that can withstand convection reflow soldering without damage. Some manufacturers have developed processes to thermally set the well known PET dielectric at the molecular level and produce chip capacitors suitable for reflow use up to 220°C. However, most film chip producers lack this technology and have rushed into developments using higher temperature film dielectrics such as PEN and PPS. The objective of producing a higher temperature film chip capacitors using these more exotic films has been achieved but performance and quality problems have also quickly surfaced. Field failures have shown that neither PEN nor PPS have the graceful aging characteristic of PET dielectric and can be subject to short circuit failure under certain conditions. Base film manufacturers are continuing to work on improving these and other high temperature films and someday hope to have a viable solution.

MUTUALLY EXCLUSIVE DEVELOPMENTS

The market pressure for reduced cost and size has driven capacitor design developments that are at odds with the Power Converter Industry's desire for more robust, stable and easy to handle components. The first choice of capacitor makers to increase capacitance density is to increase the dielectric constant. Increasing the "K" causes the dielectric to be less stable and more sensitive to environmental changes. The second choice to increase capacitance (and hopefully current handling) is to thin down the dielectric, bringing the electrode plates closer together. This simple effort tends to drive the voltage withstanding per thickness to higher stress levels, which in itself, lowers the inherent safety margin of the capacitor design. Dielectric thickness reduction tends to make the components physically harder to build, a situation that seldom

leads to increased quality. A third choice is to abandon known materials and processes in favor of newer materials such as base metal electrodes, polymerized electrolytes and new polymer thin films. These efforts are admirable but must be fully developed and field tested to understand the long term reliability of the new systems prior to commercial release.

STUDY OF CAPACITOR ROBUSTNESS

When determining the robustness of a capacitor it is necessary to examine both its electrical and mechanical stability.

A. Board Flexure Testing

Flexure or printed wiring board (PWB) bending is a significant source of stress that can lead to component failure. Ceramic capacitors are inherently brittle and can exhibit catastrophic failure if cracked during PWB bending if the crack propagates across opposing electrodes and there is sufficient energy present in the power supply. MLP capacitors are made with polymer films, which are not brittle under normal conditions and are more forgiving when physically stressed. The most common test procedures for this type of robustness follow EIAJ specification RC3402 where a capacitor is reflow soldered to pads on a test PWB. The assembly is mounted component face down, supported on the PWB ends and bending stress is applied to the backside of the assembly with a ram directly behind the component under test. The basic setup is shown in Figure 14. Capacitance shift is used to detect failure under test conditions but this may not detect cracking of ceramic capacitors. The standard also uses a 1mm deflection as an acceptance level for no failures. A test PWB with 1mm of deflection is also shown in Fig. 14. A maximum deflection of only 1mm is difficult to achieve at every step of PWB assembly and final product manufacturing to eliminate flexure cracking of ceramic capacitors. Fig 15 shows some typical results of flexure testing on ceramic and MLP capacitors.

Board Flexure Comparison between Surface Mount Multi-layer Ceramic and Film Capacitors

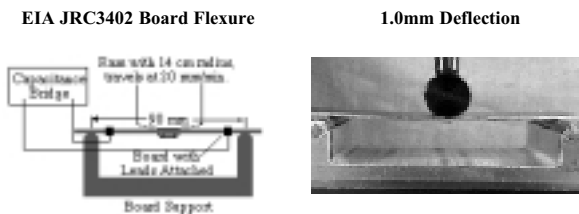


Fig. 14 Board Flexure

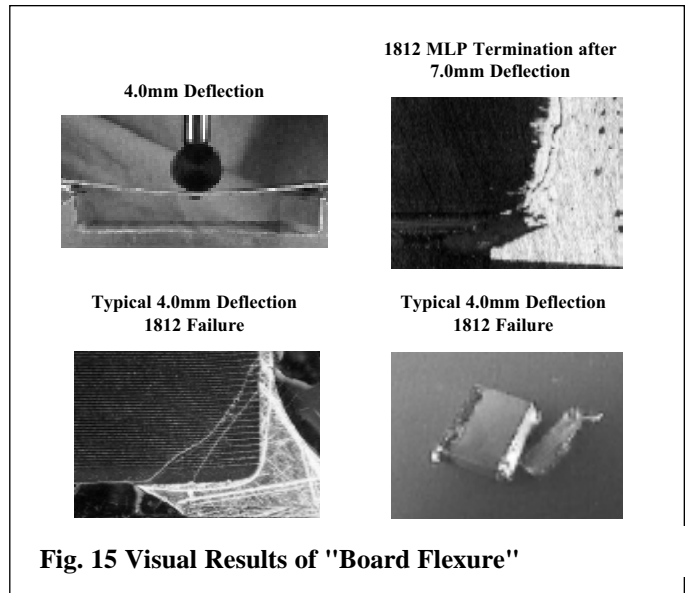


Fig. 15 Visual Results of "Board Flexure"

Flexure testing has found that while all 1812 ceramic chip capacitors tested in this particular test set failed between 3.0 and 4.0mm of deflection, MLP chip capacitors flexed at 7.0mm and subjected to 500 hours of accelerated life testing showed no failures or degradation (See Fig. 16). Throughout the testing, it was evident that MLP capacitors did not exhibit

Post Board Flexure MLP Life Test Data Summary after 500 Hours at 125°C and 100V DC

Part Number	Parameter	Limit/Actual Average
224K100ST1812	% Delta Cap	5.00/2.1
	% DF	1.00/0.55
	IR (Meg Ohm)	1000/100,000
105K100ST2824	% Delta Cap	5.00/1.75
	% DF	1.00/0.51
	IR (Meg Ohm)	1000/70,000
225K100ST3827	% Delta Cap	5.00/1.91
	% DF	1.00/0.54
	IR (Meg Ohm)	454/15,000
105K100ST3	% Delta Cap	5.00/3.09
	% DF	1.00/0.55
	IR (Meg Ohm)	1000/100,000
405K100CB4	% Delta Cap	5.00/2.28
	% DF	1.00/0.54
	IR (Meg Ohm)	250/12,000

Fig. 16 MLP "Board Flexure" Robustness

failure or degradation when tested at or beyond deflection values that cracked ceramic capacitors of similar size and values. The testing also indicated that the use of gull wing and J lead surface mount capacitors of either type survived test PWB deflection without degradation or failure.

B. Temperature Coefficient of Expansion

Placement of chips on PWBs via reflow soldering requires that the coefficients of expansion of the various materials be close enough that the expansion stresses do not cause failures to occur. An analysis of the various CTEs shows why large chip capacitors are so prone to failure. Figure 17 shows that MLP capacitors and FR4 boards have virtually identical CTEs.

CTEs	
On Typical Components and Substrates	
<u>Material</u>	<u>CTE (ppm/°C)</u>
Ceramic Capacitor	9.5-11.5
Alumina	≈7
Copper	17.6
Copper Clad Invar	6-7
Filled Epoxy Resin	18-25
FR-4 PC Board	≈18
Nickel or Steel	≈15
Polyimide/Class PCB	≈12
Polyimide/Kelvar PCB	≈7
Tantalum	6.5
Tin Lead Alloys	≈27
MLP "Polymer" Capacitor	≈17

CTE - Coefficient of Thermal Expansion a.k.a. TEC

Fig. 17 Typical Coefficient of Thermal Expansions

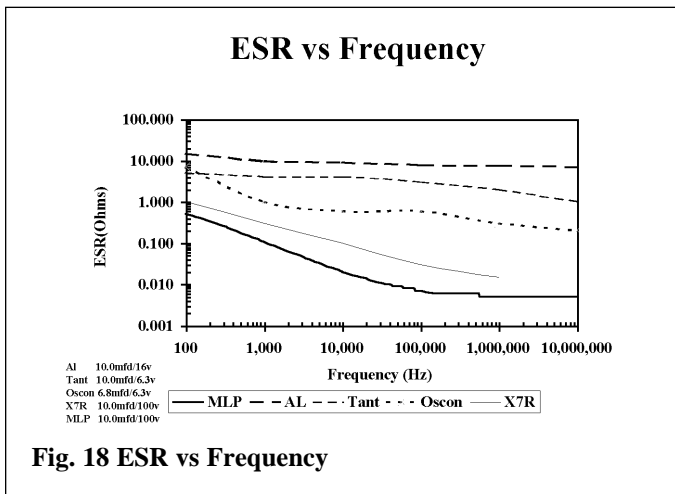


Fig. 18 ESR vs Frequency

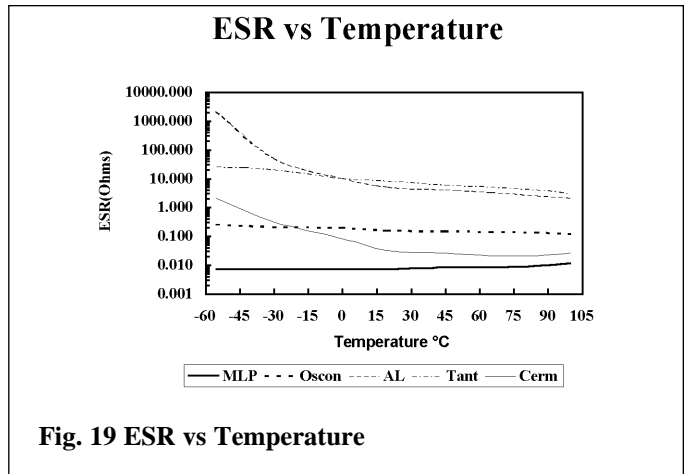


Fig. 19 ESR vs Temperature

C. ESR Stability

One of the most important attributes of a capacitor used in power circuits is its Equivalent Series Resistance (ESR). ESR determines the I²R heating losses for the capacitor, which in turn establishes the efficiency, pulse handling and indirectly the reliability of the circuit. Figures 18 and 19 show comparisons of the ESR of various dielectric systems and how they vary with temperature and frequency.

The charts in Figures 18 and 19 show that MLP capacitors, in terms of "high valued" capacitance and small package size, represent the lowest ESR valued capacitors available.

Figures 20, 21 and 22 show comparisons between ceramic and MLP capacitors for the critical parameters of dissipation factor (capacitor losses) and change of capacitance under DC bias and temperature variation.

CONCLUSION

With DATACOM applications seeking to achieve the 5x9 (99.999%) up time reliability levels required for most TELECOM applications, the choice of the proper components used in high-density power converters has become more crucial than ever. Instead of using capacitors that simply get by, critical applications require units with an established track record of both durability and reliability. The TELECOM industry learned decades ago that while the other capacitor technologies have their viable uses, in pivotal applications only metallized film capacitors have the inherent performance, stability and reliability needed. With their ultra-low ESR, outstanding power handling capabilities and small package size, MLP capacitors are positioned to see increased use in these leading edge type applications.

REFERENCES

- [1] Kemet Web page: Product Information, Kemet Electronics Corporation, <http://www.kemet.com>, copyright 1999.
- [2] Capacitor Insulation, Wiley Encyclopedia of Electrical and Electronics Engineering, Vol. 3, 1999
- [3] W. J. Sarjeant, Capacitor fundamentals, Proc. 1989 IEEE Electr. Insulation Conf., Chicago, IL, 1989, pp. 1-51.
- [4] J. D. Prymak, Tantalum Ultra-Low ESR Developments for SMPS Applications, Kemet Application Bulletin, <http://www.kemet.com>, 1998.
- [5] J. Maxwell, Board Flexure Comparison between Surface Mount Multi-layer Ceramic and Film Capacitors, Presentation at CARTS '99, March 15-19, 1999.
- [6] L. Mann & J. Beeson, Advances in "Low-Fire" Dielectric Technology for the Manufacture of MLCC and Comparison with Base Metal Electrode Technology, Presentation at CARTS '2000, March 16-20, 2000.

% Dissipation Factor vs Vrms

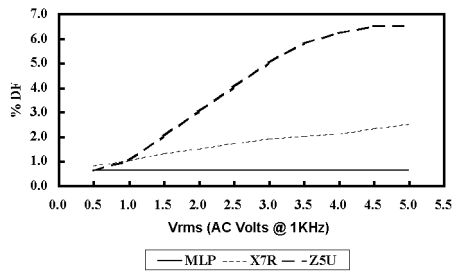


Fig. 20 % Dissipation Factor vs Vrms

% Capacitance Change vs DC Bias

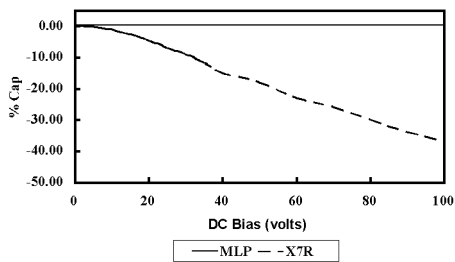


Fig. 21 % Capacitance Change vs DC Bias

% Capacitance Change vs Temperature

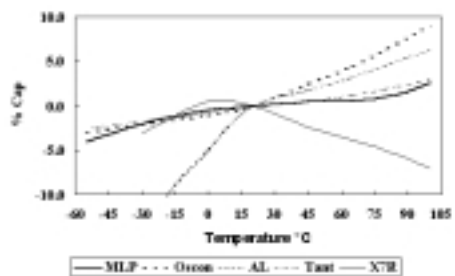


Fig. 22 % Capacitance Change vs Temperature